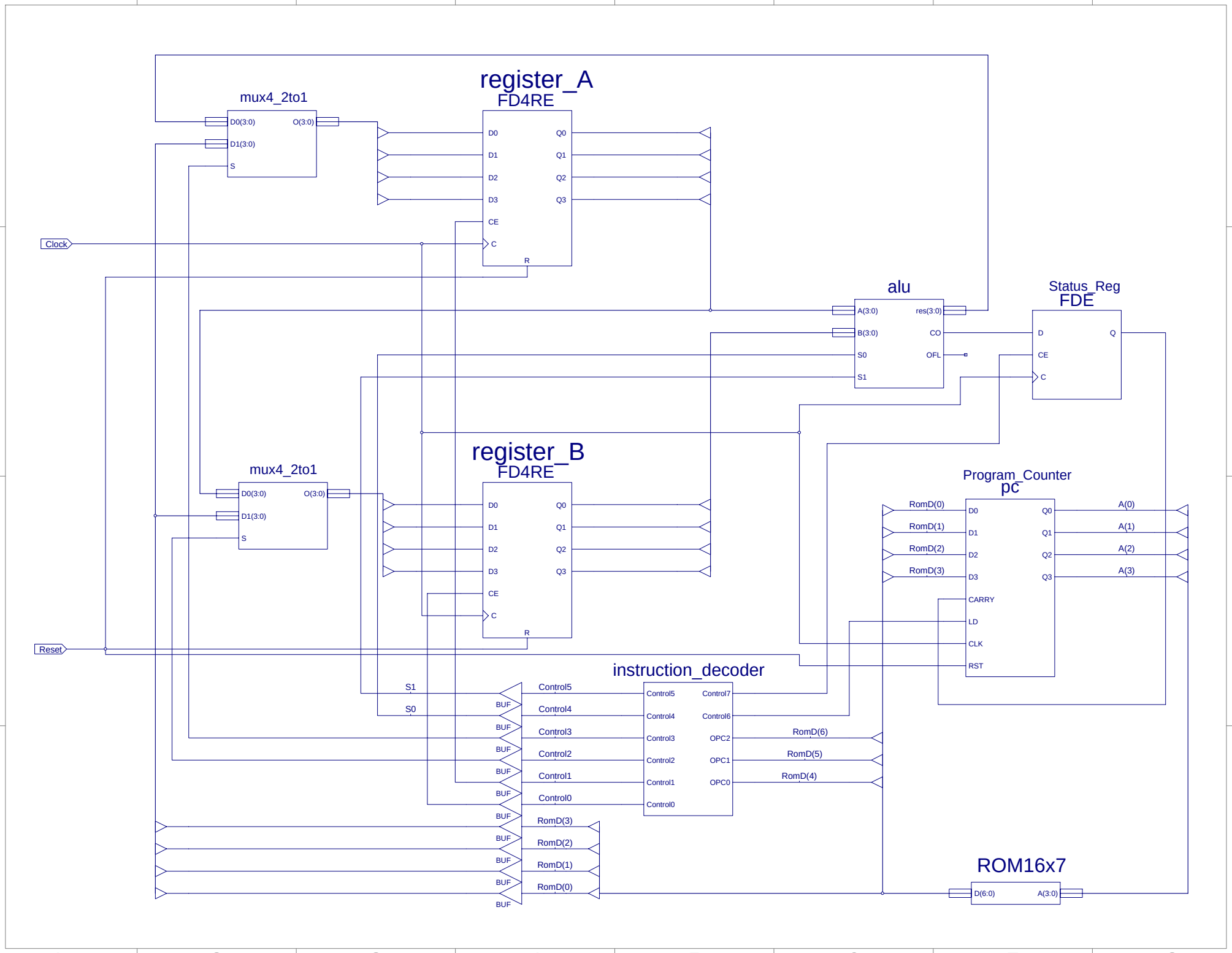
register_A
FD4RE
mux4_2to1
D0(3:0)
O(3:0)
D1(3:0)
S
D0
D1
D2
D3
CE
C
R
Q0
Q1
Q2
Q3
Clock
alu
A(3:0)
B(3:0)
S0
S1
res(3:0)
CO
OFL
Status_Reg
FDE
D
CE
C
Q
register_B
FD4RE
mux4_2to1
D0(3:0)
O(3:0)
D1(3:0)
S
D0
D1
D2
D3
CE
C
R
Q0
Q1
Q2
Q3
Program_Counter
pc
RomD(0)
RomD(1)
RomD(2)
RomD(3)
D0
D1
D2
D3
CARRY
LD
CLK
RST
Q0
Q1
Q2
Q3
A(0)
A(1)
A(2)
A(3)
Reset
instruction_decoder
S1
S0
BUF
Control5
Control4
Control3
Control2
Control1
Control0
Control7
Control6
OPC2
OPC1
OPC0
RomD(6)
RomD(5)
RomD(4)
RomD(3)
RomD(2)
RomD(1)
RomD(0)
ROM16x7
D(6:0)
A(3:0)