## Answers Homework 4

1) A combinatorial circuit is defined by the following three Boolean functions.

$$
\begin{aligned}
& \mathrm{F} 1=(\mathrm{X}+\mathrm{Z})^{\prime}+\mathrm{XYZ} \\
& \mathrm{~F} 2=(\mathrm{X}+\mathrm{Z})^{\prime}+\mathrm{X}^{\prime} \mathrm{YZ} \\
& \mathrm{~F} 3=\mathrm{XY}^{\prime} \mathrm{Z}+(\mathrm{X}+\mathrm{Z})^{\prime}
\end{aligned}
$$

Design a circuit with a single decoder and external OR gates.

Our combinational circuit has 3 inputs ( $\mathrm{X}, \mathrm{Y}, \mathrm{Z}$ ) and 3 outputs (F1, F2, F3). So, we can implement it using one 3-to-8 Decoder. In order to do this we first need to find the minterms of each function. So we convert to CSOP.

$$
\begin{aligned}
\mathrm{F} 1 & =(\mathrm{X}+\mathrm{Z})^{\prime}+\mathrm{XYZ} \\
& =\mathrm{X}^{\prime} Z^{\prime}+\mathrm{XYZ}=\mathrm{X}^{\prime} \mathrm{Z}^{\prime}\left(\mathrm{Y}+\mathrm{Y}^{\prime}\right)+\mathrm{XYZ} \\
& =\mathrm{X}^{\prime} \mathrm{Y}^{\prime} \mathrm{Z}^{\prime}+\mathrm{X}^{\prime} \mathrm{YZ}+\mathrm{XYZ} \\
& =\mathrm{m} 0+\mathrm{m} 2+\mathrm{m} 7
\end{aligned}
$$

$$
\begin{aligned}
\mathrm{F} 2 & =(\mathrm{X}+\mathrm{Z})^{\prime}+\mathrm{X}^{\prime} \mathrm{YZ} \\
& =\mathrm{X}^{\prime} \mathrm{Z}^{\prime}+\mathrm{X}^{\prime} \mathrm{YZ}=\mathrm{X}^{\prime} \mathrm{Z}^{\prime}\left(\mathrm{Y}+\mathrm{Y}^{\prime}\right)+\mathrm{X}^{\prime} \mathrm{YZ} \\
& =\mathrm{X}^{\prime} \mathrm{Y}^{\prime} \mathrm{Z}^{\prime}+\mathrm{X}^{\prime} Y Z Z^{\prime}+\mathrm{X}^{\prime} Y Z \\
& =\mathrm{m} 0+\mathrm{m} 2+\mathrm{m} 3
\end{aligned}
$$

$$
\begin{aligned}
\mathrm{F} 3 & =X Y^{\prime} Z+(X+Z)^{\prime} \\
& =X Y^{\prime} Z+X^{\prime} Z^{\prime}=X Y^{\prime} Z+X^{\prime} Z^{\prime}\left(Y+Y^{\prime}\right) \\
& =X Y^{\prime} Z+X^{\prime} Y^{\prime} Z+X^{\prime} Y Z^{\prime} \\
& =m 5+m 0+m 2
\end{aligned}
$$

Now we know which outputs of the decoder we need to OR in order to implement each function. For F1 we have to OR outputs 0 , 2, and 7 . For F2 we have to OR outputs 0, 2, and 3. For F3 we have to OR outputs 0, 2, and 5.

Now we get the following implementation of our combinational circuit.

2) Implement a binary full adder with a single 4-to-1 2-line multiplexer and a single inverter.

| Cin | A | B | S $(\mathrm{A}+\mathrm{B})$ | Cout |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 | 0 | S = B |
| 0 | 0 | 1 | 1 | 0 | Cout $=0$ |
| 0 | 1 | 0 | 1 | 0 | S = B |
| 0 | 1 | 1 | 0 | 1 | Cout $=$ B |
| 1 | 0 | 0 | 1 | 0 | S = B |
| 1 | 0 | 1 | 0 | 1 | Cout $=$ B |
| 1 | 1 | 0 | 0 | 1 | S = B |
| 1 | 1 | 1 | 1 | 1 | Cout $=1$ |



