CURRICULUM VITAE
of
TODOR STEFANOV

PERSONAL:

Date of Birth:	11 July 1974
Place of Birth:	Samokov, Bulgaria
Nationality:	Bulgarian
Marital Status:	Married, two children
Personal Web Page:	http://www.liacs.nl/~stefanov/

CONTACT INFORMATION:

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EDUCATION

2000-2004	**Ph.D. in Computer Science,** (degree awarding date: 14 December 2004) Leiden Institute of Advanced Computer Science (LIACS), Faculty W&N, Leiden University, The Netherlands
Thesis title:	"*Converting Weakly Dynamic Programs to Equivalent Process Network Specifications*"
Supervisor:	Prof. dr. Ed Deprettere
1993-1998	**M.Sc., Computer Systems Engineering,** GPA 5.87/6.00, in top 5% of the class Faculty of Computer Systems and Control, Technical University of Sofia, Bulgaria
Thesis title**:**	*"Design, Analysis, and Area Minimization of the Control Unit of Application Specific Microprocessor Core"*
Supervisors:	Prof. dr. Angel Popov, Prof. dr. Peter Manoilov
1988-1993	**Specialist in Microprocessor Engineering,** GPA 5.94/6.00, in top 5% of the class Vocational High Technical School of Microprocessor Engineering with Teaching of English Language, Pravetz, Bulgaria
Thesis title:	*"Design of Distributed Data Base Using Several Microcomputers"*
Supervisor:	Prof. dr. Stoyan Bonev (Technical University of Sofia)

EMPLOYMENT

Sept. 2008 – present	*Leiden Embedded Research Center (LERC)*, Leiden Institute of Advanced Computer Science (LIACS), Faculty W&N, Leiden University, The Netherlands
Position:	Assistant Professor
Sept. 2007 – Aug. 2008	*Computer Engineering Laboratory*, Faculty of Electrical Engineering, Mathematics, and Computer Science, Delft University of Technology, The Netherlands
Position:	Senior Researcher
Projects:	hArtes (FP6 EU project, http://www.hartes.org) – overall budget 17 000 000 euro;
June 2004 – Aug. 2007	*Leiden Embedded Research Center (LERC)*, Leiden Institute of Advanced Computer Science (LIACS), Faculty W&N, Leiden University, The Netherlands
Position:	Postdoctoral Researcher

Projects:	ARTEMISIA (STW project LES.6389, http://artemisia.liacs.nl) – overall budget 1 825 000 euro; DAEDALUS (STW/Progress+ project, http://daedalus.liacs.nl) – overall budget 85 000 euro;
May 2000 – May 2004	*Leiden Embedded Research Center (LERC)*, Leiden Institute of Advanced Computer Science (LIACS), Faculty W&N, Leiden University, The Netherlands
Position:	Research Assistant
Projects:	ARTEMIS (STW/Progress project AES.5021, http://ce.et.tudelft.nl/artemis/) – overall budget 2 500 000 euro; COMPAAN/LAURA (sponsored by LIACS, www.liacs.nl/~cserc/compaan/) – overall budget N.A.
Industrial Impact:	Ideas from my doctoral research have been moved successfully for commercialization to a start-up company called Compaan Design BV (www.compaandesign.com). This was done with a 200 000 EUR valorization grant from the Dutch Technology Foundation STW.
Dec. 1997 - May 2000	"*Innovative Micro Systems*" Ltd., Sofia, Bulgaria
Positions:	Research and Development Engineer (since July 1998) Research and Development Technical Assistant (until June 1998)
Projects:	*MSOS ICE* - MicroSystems-on-Silicon In-Circuit Emulator; *Rapido8E* - Microprocessor with Cost-Efficient RISC Architecture; *Intellectual Property (IP) cores* – development of Synthesizable VHDL models; *Application-Specific Microprocessor Design* – Architecture and Organization (FPGA and ASIC prototyping).
Activities:	Involved in the design of a high-performance, reconfigurable MicroSystems-on-Silicon In-Circuit Emulator; Developed hardware and processor cores with critical area and performance constraints that had been included in the digital IP library of the company.
Expertise:	- Hardware/software co-design - Embedded systems design - Design of systems on FPGAs - IP cores design: synthesizable VHDL for ASIC and FPGA - Assembler language programming of microcontrollers and microprocessors
Jan. 1995 – Dec. 1997	"*ELSIEL*" Ltd., Sofia, Bulgaria
Position: Expertise:	HW/SW Designer of Digital Electronic Devices - Controllers for power electronic devices (such as UPSs, Generators, etc.) - Embedded microcontrollers programming - Applications based on microcontrollers and microprocessors

PUBLICATION SUMMARY

Publications in journals and conferences

I have (co-)authored 61 scientific publications. For a detailed list of my publications, see **Appendix A**. My publication list includes 2 books (peer reviewed), 12 international journal papers (all peer reviewed) and 47 international conference papers (all peer reviewed).

Quality of my journal papers. Five of my journal papers, see [3],[5],[9],[10],[12] in Appendix A, are in some of the top international journals in my field of research: 1) papers [9] and [12] are in the top international journal for computer aided design called *IEEE Transactions on Computer-Aided Design of Integrated Circuits and*

Systems (TCAD); 2) papers [3] and [5] are in the top international journal for embedded systems called *ACM Transactions on Embedded Computing Systems (TECS)*; 3) paper [10] is in the top international journal for reconfigurable computing called *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*. Moreover, my journal paper [12] is:

- **WINNER of the prestigious international 2009 DONALD O. PEDERSON BEST PAPER AWARD!** (http://www.ece.umn.edu/~sachin/tcad/best_paper_award.html)
- **TOP 10th downloaded article of the international journal IEEE TCAD for 2009!** (http://tcad.polito.it/editor/Top_2009CAD.html)
- **TOP 7th downloaded article of the international journal IEEE TCAD for 2008!** (http://tcad.polito.it/editor/Top_2008CAD.html)

Quality of my conference papers. Many of my conference papers have been published and presented at the top international conferences in my field of research such as Design Automation Conference (DAC), Design Automation and Test in Europe (DATE), Int. Conf. on Hardware/Software Co-Design and System Synthesis (CODES+ISSS), Int. Conf. on Embedded Software (EMSOFT), Int. Conf. on Computer Aided Design (ICCAD), and Int. Conf. on Field Programmable Logic and Applications (FPL). Each of these top conferences has a very tough peer review process with *paper acceptance rate below 25%* from a total number of paper submissions between 300 and 1000. Moreover, a few of my conference papers have been acknowledged as follows:

- My DAC 2013 paper [16] is the **WINNER of the 2013 HiPEAC PAPER AWARD!**
- My DAC 2011 paper [26] is the **WINNER of the 2011 HiPEAC PAPER AWARD!**
- My ESTIMedia 2010 paper [27] is the **WINNER of the 2010 ESTIMedia BEST PAPER AWARD!**
- My EMSOFT 2011 paper [24] was **NOMINATED for the 2011 EMSOFT BEST PAPER AWARD!**
- My DATE 2010 paper [30] was **NOMINATED for the 2010 DATE BEST PAPER AWARD!**
- My CODES+ISSS 2006 paper [46] is **MOST HIGHLY-CITED CODES/ISSS PAPER/IDEA for 2006! (see http://portal.acm.org/citation.cfm?id=1450178).**

Citation-trend analysis after the promotion.

My citation index has increased significantly after my PhD promotion. Currently, my **H-index is 14** and my **G-index is 32**. I used the most popular publicly available tool for citation analysis called “Publish or Perish”:

Harzing, A.W. (2007) ***Publish or Perish****, available from http://www.harzing.com/pop.htm*

This tool uses the Google Scholar database for publications and citations. I ran the tool with a query “Todor Stefanov” – see in **Appendix B** a snapshot from the tool with the citation analysis results for my publications**.** Below, I provide a summary of the results:

Papers:	60	Cites/paper:	17.75	**h-index:**	**14**	AWCR:	145.49
Citations:	1065	Cites/author:	320.25	**g-index:**	**32**	AW-index:	12.06
Years:	14	Papers/author:	20.53	hc-index:	12	AWCRpA:	43.94
Cites/year:	76.07	Authors/paper:	3.28	hI-index:	4.26	e-index:	26.23
				hI,norm:	11	hm-index:	7.78

Query date: 2013-04-21

Hirsch a=5.43, m=1.00
Contemporary ac=4.04
Cites/paper: 17.75/5.0/0 (mean/median/mode)
Authors/paper: 3.28/3.0/3 (mean/median/mode)

2 paper(s) with 1 author(s)
9 paper(s) with 2 author(s)

25 paper(s) with 3 author(s)
18 paper(s) with 4 author(s)
6 paper(s) with 5 author(s)

Interpreting the data above depends very much on the field of research and many other factors. For example, in my field of research "Embedded Systems and Software" usually a person becomes a Full Professor with an h-index of 15 or higher.

Publications with researchers from outside my own research group

I have around 16 papers, see [6][9][10][22][25][32][35][36][37][38][39][41][43][44][47][57] in Appendix A, published with colleagues from USA, Europe, and The Netherlands all outside my own research group. Moreover, my IEEE journal paper [9] and the IEEE conference papers [43][44][47] have been published in cooperation with some of the top scientists in my field of research, namely Prof. Daniel Gaijski (University of California at Irvine, USA), Prof. Juergen Teich (University of Erlangen-Nurmberg, Germany), Prof. Stamatis Vassiliadis (TU Delft, The Netherlands), Prof. Lothar Thiele (ETH, Zurich, Switzerland), and Prof. Shuvra Bhattacharyya (University of Maryland at College Park, USA);

EXPERIENCE IN SUPERVISING PHD STUDENTS and POSTDOCS

Number of PhD students and PostDocs:

At Leiden University, I have already supervised and successfully promoted 3 PhD students as well as I have supervised 2 PostDocs. Currently, I am the supervisor and promotor of 6 PhD students. The list below provides information about my former and current PhD students and PostDocs.

Former PhD students:

1. **Hristo Nikolov**
   Title of PhD Thesis: *"System-Level Design Methodology for Streaming Multi-Processor Embedded Systems"*
   Date of Promotion: *April 16, 2009*
   First Job after graduation: *PostDoc Researcher, LIACS - Leiden University, The Netherlands*
   For more info see: www.liacs.nl/~nikolov
2. **Sjoerd Meijer**
   Title of PhD Thesis: *"Transformations for Polyhedral Process Networks"*
   Date of Promotion: *December 8, 2010*
   First Job after graduation: *Compiler Engineer at ACE Associated Compiler Experts B.V., The Netherlands*
   For more info see: http://www.liacs.nl/~smeijer/
3. **Dmitry Nedezhkin**
   Title of PhD Thesis: *"Parallelizing Dynamic Sequential Programs using Polyhedral Process Networks"*
   Date of Promotion: *December 20, 2012*
   First Job after graduation: *AT Consulting, Moscow, Russia*
   For more info see: http://www.liacs.nl/~dmitryn

Former PostDocs:

1. **Dr. Hristo Nikolov**
   Time Period: *from July 2009 until July 2012*
   For more info see: http://www.liacs.nl/~nikolov

2. **Dr. Sven Verdoolaege**
   Time Period: *from July 2011 until July 2012*
   For more info see: http://www.liacs.nl/~sverdool

Current PhD students:

1. **Mohamed Bamakhrama**
   Title of PhD Thesis: *TBD*
   Date of Promotion: *expected in December 2013*
   First Job after graduation: *n.a.*
   For more info see: http://www.liacs.nl/~mohamed
2. **Teddy Zhai**
   Title of PhD Thesis: *TBD*
   Date of Promotion: *expected in July 2014*
   First Job after graduation: *n.a.*
   For more info see: http://www.liacs.nl/~tzhai
3. **Emanuele Cannella**
   Title of PhD Thesis: *TBD*
   Date of Promotion: *expected in December 2014*
   First Job after graduation: *n.a.*
   For more info see: http://www.liacs.nl/~cannella
4. **Mohammad Al Hissi**
   Title of PhD Thesis: *TBD*
   Date of Promotion: *expected in May 2015*
   First Job after graduation: *n.a.*
   For more info see: http://www.liacs.nl/~alhissi
5. **Jelena Spasic**
   Title of PhD Thesis: *TBD*
   Date of Promotion: *expected in December 2015*
   First Job after graduation: *n.a.*
   For more info see: http://www.liacs.nl/~jspasic
6. **Di Liu**
   Title of PhD Thesis: *TBD*
   Date of Promotion: *expected in January 2016*
   First Job after graduation: *n.a.*
   For more info see: http://www.liacs.nl/~dliu

At Technical University of Delft, I have supervised 3 PhD students and significantly contributed for their successful graduation and promotion. The list below provides information about my former PhDs at the Computer Engineering Laboratory in TU Delft:

1. **Zubair Nawaz**
   Title of PhD Thesis: *"Recursive Variable Expansion a transformation for Reconfigurable Computing"*
   Date of Promotion: January *2011*
   First Job after graduation: *PostDoc at Delft University of Technology*
   For more info see: http://ce.et.tudelft.nl/~zubair/
2. **Jae Yong Hur**
   Title of PhD Thesis: *"Customizing and Hardwiring On-chip Interconnects in FPGAs"*
   Date of Promotion: February 28, *2011*
   First Job after graduation: *Senior Engineer at Samsung Electronics in Korea*
   For more info see: http://ce.et.tudelft.nl/~jyhur/

3. **Ozana Silvia Dragomir**
   Title of PhD Thesis: *"K-loops: Loop Transformations for Reconfigurable Architectures"*
   Date of Promotion: *July 2011*
   First Job after graduation: *n.a.*
   For more info see: http://ce.et.tudelft.nl/~ozanad/

Quality of PhD students and PostDocs:

The quality of my PhD students and PostDocs is at the highest international and national levels. All their research work has been published at top international peer-reviewed journals and conferences. Moreover:

- My current PhD student Mohamed Bamakhrama has been awarded the **ACM SIGBED 2011 Frank Anger Memorial Award given by the International Special Interest Group on Embedded Systems;**
- The PhD research work of my former PhD student Hristo Nikolov has been nominated for: **"Discovery of the Year 2009 of the Faculty of Science, Leiden University"** and **"Top 10 talents for the Simon Stevin Gazel Prize of STW in 2010"**.
- The PhD research work of my former PhD student Dmitry Nadezhkin attracted the attention and interest of Intel Corporation. As a consequence, Intel sponsored further development of the research ideas in a form of a research grant.

EXPERIENCE IN GETTING RESEARCH FUNDING AND WRITING PROPOSALS

Number of subsidies obtained for PhD students and PostDocs

Since I started my tenure track in 2008, I have acquired **7 research grants** (2 EU, 3 STW, 1 NWO, 1 Intel Corporation) with a total net funding for LIACS – Leiden University of around **€ 1 520 000**. With this funding I was able **to appoint 7 PhDs, 2 PostDocs, and 2 scientific programmers** in my research group. In addition, I have written small research proposals for 2 students who received, based on these proposals, **2 PhD scholarships** with a total amount of around **€ 124 000** from the Dutch organization Nuffic and the China Scholarship Council to pursue a PhD degree in my group. Below, I provide a detailed list of the research grants and scholarships acquired by me for PhDs and PostDocs:

Project Title: "*SCALOPES: Scalable Low Power Embedded Systems*"
Funding Organization: *EU commission / FP7 / ARTEMIS JU*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 432 000*
Project Duration: *Jan 2009 until Mar 2011*
PostDocs: *Hristo Nikolov*
PhDs: *Mohamed Bamakhrama, Mohamed Al Hissi, Sven van Haastreght*

Project Title: "*MADNESS: Methods for Predictable Design of Heterogeneous Embedded Systems with Adaptivity and Reliability Support*"
Funding Organization: *EU commission / FP7*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 247 352*
Project Duration: *Jan 2010 until Jan 2014*
PhD: *Emanuele Cannella*

Project Title: "Energy Efficient Computer-Brain Interaction"
Funding Organization: *STW Open Competition*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 217 500*
Project Duration: *Oct 2013 until Oct 2017*
PhD: *To be appointed*

Project Title: "*NEST: Netherlands Streaming*"
Funding Organization: *STW Open Competition*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 230 532*
Project Duration: *Nov 2009 until Nov 2013*
PhD: *Teddy Zhai*

Project Title: "*Daedalus: Artemisia's Open Source Framework*"
Funding Organization: *STW / program PROGRESS+*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 70 000*
Project Duration: *Nov 2008 until July 2010*
Scientific Programmers: *Stoyan Boshev and Hristo Shekov*

Project Title: *"CREED: Cross-layer Design Space Exploration for Energy-aware MP-SoC Design"*
Funding Organization: *NWO Open Competition*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 218 693*
Project Duration: *Sept 2011 until Sept 2015*
PhD: *Jelena Spasic*

Project Title: *"Automated Parallelization of Dynamic Applications for MPSoC Design and Programming"*
Funding Organization: *Intel Corporation / Intel Academic Research Office*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *$ 150 000*
Project Duration: *July 2011 until July 2012*
PostDocs: *Hristo Nikolov and Sven Verdoolaege*

Project Title: *"Analysis and Design of Adaptive Embedded Systems-on-Chip"*
Funding Organization: *China Scholarship Council*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 57 600*
Project Duration: *Sept 2011 until Sept 2015*
PhD: *Di Liu*

Project Title: *"Investigation, evaluation, and implementation of a fault tolerant programming model for distributed environment"*
Funding Organization: *Nuffic / Netherlands Fellowship Program*
Principal Investigator for LIACS: *Todor Stefanov*
Net Funding for LIACS: *€ 65 210*
Project Duration: *Sept 2011 until Sept 2015*
PhD: *Herve Kabamba*

Involvement in projects which are internationally externally financed

I have been involved in 5 large EU funded projects and 2 company funded projects by Intel and Google. My degree of involvement is as follows:

- Project Leader for LIACS in the SCALOPES EU project (http://www.scalopes.eu/);
- Project Leader for LIACS and Work Package Leader in the MADNESS EU project (http://www.madnessproject.org/);
- Project Leader for LIACS in the TSAR EU project (http://www.catrene.org/web/downloads/profiles_medea/2A718-TSAR-profile-outMEDEA2%20(23-6-10).pdf);
- Project Leader for LIACS in the SoftSoc EU project (http://www.softsoc.org/);
- Senior Researcher in the hArtes EU project (http://hartes.org/hArtes/);
- Project Leader for LIACS in the Intel project;

- Senior Researcher in the Google project;

Access to important (inter)national facilities

I have been contributing to the proposal for the latest constellation of the DAS-4 cluster super computer (http://www.cs.vu.nl/das4/) that is realized and run by several Dutch institutions (VU, LIACS, UvA, TUD, and ASTRON). In particular, I have proposed how the LIACS part of the DAS-4 cluster could be extended with FPGA nodes. LIACS has received access and funding to extend the DAS-4 cluster.

TEACHING EXPERIENCE

2005 – now	*Main Lecturer* of the course *"Digital Technique"* at LIACS, Leiden University. Designed and developed this course which consists of 15 lectures (each 3 academic hours), 4 hands-on tutorials, 1 design project (design, simulation, synthesis, and FPGA prototyping of a 4-bit microprocessor), and 8 homework assignments. For more details see: http://www.liacs.nl/~stefanov/courses/DITE/
2010 – now	Main *Lecturer* of the course *"Embedded Systems and Software"* at LIACS, Leiden University. Designed and developed this course which consists of 10 lectures (each 2 academic hours), and 5 hands-on sessions (design, simulation, synthesis, and FPGA prototyping of a Multi-processor System-on-Chip). For more details see: http://www.liacs.nl/~stefanov/courses/ES/
2003 – 2007	*Assistant Lecturer and Tutor* in the course *"Embedded Systems and Software"* at LIACS, Leiden University. Webpage: www.liacs.nl/~cserc/EMBSYST/EMBSYST2007/EMBSYST2007.html
2000 – 2004	*Teaching Assistant and Tutor* in the course *"Digital Technique"* at LIACS, Leiden University.
1998 – 2000	*Tutorials* conducted at the Technical University of Sofia. *Course name*: "Principles of VLSI Design, Synthesis and Simulation". *Course synopsis*: Digital Circuit Design with Hardware Description Languages (VHDL, Verilog). *Course duration*: one term. *Number of students:* two groups, each with around 10 students. *Course specifics:* The tutorials took place at "*Innovative Micro Systems*" Ltd., Sofia, Bulgaria in a real chip production industrial environment, including clean-room facilities and a production line.

INTERNATIONAL VISIBILITY

Invited speaker at international conferences and other forums

I have given around 16 invited talks including 2 talks at the top international conferences in my field of research, namely the Design Automation Conference (DAC, www.dac.com) and the Design, Automation and Test in Europa (DATE, www.date-conference.com). Below, I provide a detailed list with my invited talks:

1. "Challenges in Mixed-Criticality Embedded Systems Design", *European Space Agency – European Space Research and Technology Center (ESA-ESTEC)*, Noordwijk, The Netherlands, September 21, 2012.
2. "A Methodology for Automated Design of Hard-Real-Time Embedded Streaming Systems", *Intel Research Laboratories*, St. Petersburg, Russia, May 28, 2012.

3. "Daedalus: Toward Composable Multimedia MP-SoC Design", *Design Automation Conference (DAC)*, Anaheim, USA, June 11, 2008.
4. "Making System-level Design Take off", *Design, Automation and Test in Europe Conference (DATE)*, Nice, France, May 24, 2009.
5. "Towards Composable System-level Design of Multimedia MP-SoCs", *Intel Research Laboratories*, St. Petersburg, Russia, November 2, 2010.
6. "ESPAM: Embedded System-level Platform synthesis and Application Mapping (with Demo!)", *European Space Agency – European Space Research and Technology Center (ESA-ESTEC)*, Noordwijk, The Netherlands, November 29, 2006.
7. "Algorithmic Transformation Techniques for Efficient Exploration of Alternative Application Instances", *Berkeley Wireless Research Center (BWRC), University of California at Berkeley*, USA, May 10, 2002.
8. "Algorithmic Transformation Techniques for Exploration of Alternative Application Instances", *Institute of Micro Electronics (IMEC),* Leuven, Belgium, April 19, 2002.
9. "Y-Chart Based System Level Performance Analysis: an M-JPEG Case Study", *NATLAB - Philips Research Laboratories*, Eindhoven, The Netherlands, September 29, 2000.
10. "Automated Derivation of Process Networks", *ASCI Winter School on Programming Multi-core Systems*, Soest, The Netherlands, March 17, 2010.
11. "From Sequential Application Specification to FPGA-based Heterogeneous MPSoC platform execution", *Int. Workshop on Mapping of Applications to MPSoCs*, Schloss Rheinfels, St. Goar, Germany, June 17, 2008.
12. "ESPAM: Embedded System-level Platform synthesis and Application Mapping (with Demo!)", *Hardware-Software Co-Design group at University of Erlangen-Nuremberg*, Germany, June 06, 2007.
13. "DAEDALUS: A Framework for Rapid System-level Exploration, Synthesis, and Programming of Multimedia MP-SoCs (with Demo!)", *Embedded System Architectures group at Eindhoven University of Technology*, The Netherlands, May 16, 2007.
14. "Exploring, Programming, and Prototyping of MP-SoCs within 24 hours", *Dutch Technology Foundation STW*, Utrecht, The Netherlands, August 25, 2006.
15. "The COMPAAN Tool Chain to convert Matlab into Process Networks (with Demo!)", *Computer Engineering Colloquium at Delft University of Technology*, The Netherlands, March 21, 2002.
16. "Unrolling/Skewing in Compaan", *University Louis Pasteur*, Strasbourg, France, June 20, 2001.

Involvement in the organization of seminars, workshops, and conferences

I serve on the organizational committees of almost all top conferences, symposia, and workshops in my field of research. Below, I provide a detailed list of my involvement:

- Invited for **General Chair (2015)** of the IEEE International Symposium on Embedded Systems for Real-time Multimedia (ESTIMedia);
- **Program Chair (2013 and 2014)** of the IEEE International Symposium on Embedded Systems for Real-time Multimedia (ESTIMedia);
- **Track Program Chair (2013)** IEEE/ACM/IFIP International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS);
- **Program Chair (2010)**, 13th International Workshop on Software and Compilers for Embedded Systems (SCOPES);
- **Technical Program Committee Member (2013, 2012, 2011, 2010)**, International Conference on Design, Automation and Test in Europe (DATE);
- **Technical Program Committee Member (2013, 2012, 2011, 2010, 2009, 2008, 2007)**, IEEE/ACM/IFIP International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS);
- **Technical Program Committee Member (2012)**, IEEE/ACM International Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia);
- **Technical Program Committee Member (2011),** the IEEE International Real-Time Systems Symposium (RTSS);

- **Technical Program Committee Member (2013, 2012, 2011),** 14th International Workshop on Software and Compilers for Embedded Systems (SCOPES);
- **Technical Program Committee Member (2010),** IEEE/IFIP International Conference on Very Large Scale Integration and System-on-Chip (VLSI-SoC);
- **Technical Program Committee Member (2010),** IEEE International Conference on Computer Design (ICCD);
- **Technical Program Committee Member (2013, 2012)**, International Workshop on Mapping of Applications to MPSoCs (Map2MPSoC)
- **Technical Program Committee Member (2012)**, Forum on specification and Design Languages (FDL)
- **Technical Program Committee Member (2012)**, XXI International Conference "Electronics - ET2012"

Editorial Board of international journals

I serve on the editorial board of the following international journals:

- **Associate Editor and Editorial Board Member** of the International Journal of Reconfigurable Computing;
- **Special Issue Co-Editor** of the international journal ACM Transactions on Embedded Computing Systems (TECS).

Reviewer of international scientific journals and conferences

I am a reviewer for all top international journals and conferences in my field of research. Below, I provide a detailed list of my reviewing activities.

Reviewer for International Journals:

- IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems
- IEEE Transactions on VLSI Systems
- IEEE Transactions on Signal Processing
- IEEE Transactions on Industrial Informatics
- IEEE Embedded Systems Letters
- ACM Transactions on Design Automation of Electronic Systems
- ACM Transactions on Embedded Computing Systems
- Transactions on HiPEAC
- Design Automation for Embedded Systems (Springer)
- Journal of Systems Architecture (Elsevier)
- Simulation Modeling Practice and Theory (Elsevier)
- EURASIP Journal on Embedded Systems
- EURASIP Journal on Applied Signal Processing

Reviewer for Conferences:

- Design Automation Conference (DAC) -- 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013
- Design, Automation and Test in Europe (DATE) -- 2003, 2006, 2010, 2011, 2012, 2013
- IEEE/ACM/IFIP International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS) -- 2007, 2008, 2009, 2010, 2011, 2012, 2013
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD) -- 2012
- IEEE/ACM International Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia) – 2012, 2013
- IEEE/IFIP International Conference on Very Large Scale Integration and System-on-Chip (VLSI-SoC) – 2010
- IEEE International Conference on Computer Design (ICCD) -- 2008, 2010
- IEEE International Real-Time Systems Symposium (RTSS) -- 2010

- IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP) -- 2002, 2003, 2007
- Int. Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) -- 2005
- Int. Conference on Field Programmable Logic and Applications (FPL) -- 2008
- IEEE Computer Society Annual Symposium on VLSI -- 2008
- ACM International Conference on Supercomputing (ICS) -- 2006
- ACM International Conference on Computing Frontiers (CF) – 2010
- International Workshop on Software and Compilers for Embedded Systems (SCOPES) – 2010, 2011, 2012, 2013;
- International Workshop on System Architecture, Modeling, and Simulation (SAMOS) – 2002
- International Workshop on Mapping of Applications to MPSoCs (Map2MPSoC) – 2012, 2013
- Forum on specification and Design Languages (FDL) -- 2012

MAJOR INTERNATIONA RESEARCH AND EDUCATIONAL COOPERATIONS

The DAEDALUS Research and Education Laboratory

In the beginning of 2010, I co-founded the DAEDALUS research and education laboratory, a joint laboratory between The Leiden Embedded Research Center, Leiden Institute of Advanced Computer Science, Leiden University and the Department of Electronics, Faculty of Electronic Engineering and Technology, Technical University of Sofia, Bulgaria. It is located at the campus of The Technical University of Sofia. The opening of the laboratory was on April 7, 2010 and the lab was officially opened by The Dutch Ambassador in Sofia, Bulgaria and covered by the media. The laboratory was sponsored by the DAEDALUS Foundation in The Netherlands which granted 36000 EUR to build and equip a modern 60 m^2 laboratory. Also, the laboratory was supported by the Scientific Director of LIACS (Prof. Joost Kok) and it was officially approved by the Dean of the Faculty of Science (Prof. Sjoerd Verduyn Lunel), Leiden University and the Rector of the TU-Sofia (Prof. Kamen Veselinov) by signing and exchanging official letters of support. In the laboratory, Bachelor, Master and PhD students gain theoretical and practical experience in Advanced Embedded Systems and Software Design that will help them to become highly qualified professionals in academia or industry. The Embedded Systems and Software course given by me at LIACS is officially included in the curriculum of TU-Sofia and the course has been given there every spring semester since 2010. Moreover, the laboratory serves as a platform for exchange of Bachelor, Master, and PhD students between TU-Sofia and Leiden University. In addition to that the laboratory executes joint research and development projects and will encourage the cooperation between TU-Sofia and LIACS, Leiden University in writing and participating in joint EU projects.

PROFESSIONAL MEMBERSHIPS

- Member of PhD defense committees: Vladimir Zivkovic (Leiden University, 23.09.08), Jae Young Hur (TU Delft, 28.02.11), Mojtaba Sabeghi (TU Delft, 04.04.11), Tjerk Bijlsma (University of Twente, 01.07.11), Toktam Taghavi (University of Amsterdam, 18.01.12), Mark Thomson (University of Amsterdam, 18.01.12);
- Member of the European Network of Excellence on High-Performance Embedded Architecture and Compilation (HiPEAC);
- Member of the IEEE Benelux Embedded Systems Chapter;
- Member of IEEE;
- Associate Member of the European Network of Excellence on Embedded Systems Design (ARTIST Design);
- Chairman of the DAEDALUS Foundation for research and education in Embedded Systems and Software;
- Member of the Education Committee of LIACS, Leiden University;
- Graduate School Director of LIACS, Leiden University

AWARDS, HONORS, SCHOLARSHIPS

- I'm a **recipient** of the prestigious international **2009 IEEE TCAD DONALD O. PEDERSON BEST PAPER AWARD** for my international journal article [12] "Systematic and Automated Multi-processor System Design, Programming, and Implementation" published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, No. 3, pp. 542-555, March 2008.
- I'm a **recipient** of the international **2011 HiPEAC Network of Excellence paper award** for my papers [26] published in 2011 at the top international Design Automation Conference;
- I'm a **recipient** of the international **2013 HiPEAC Network of Excellence paper award** for my papers [16] published in 2013 at the top international Design Automation Conference;
- I'm a **recipient** of the international **2010 ESTIMedia best paper award** for my paper [27] published in 2010 at the international IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia;
- I have been **nominated** for the **2011 "Discoverer of the Year"/C.J. Kok prize** of the Faculty of Science, Leiden University, The Netherlands;
- I was a **nominee** for the international **2011 EMSOFT best paper award** for my paper [24] published in 2011 at the International Conference on Embedded Software;
- I was a **nominee** for the international **2010 DATE best paper award** for my paper [30] published in 2010 at the top international Design, Automation and Test in Europe Conference;
- I was awarded a **Gratitude Bonus** in 2010 by LIACS - Leiden University for excellence in acquiring EU research funding;
- I was awarded a **Gratitude Bonus** 3 times (2003 - 2006) by LIACS - Leiden University for excellence in research;
- I received **Post Doctoral Scholarship** from PROGRESS, the embedded systems research program of the Dutch Technology Foundation STW (project LES.6389). It was worth of 153 000 euro and supported a three-years-long (2004 -- 2007) individual Post Doctoral research at LIACS, Leiden University;

Appendix A

PUBLICATIONS

Books (peer reviewed)

[1] **Todor Stefanov**, Ed Deprettere, Hristo Nikolov, Marin Marinov, and Angel Popov
"Embedded Systems: components, modeling, design and case studies",
First Edition published by Publishing House of TU-Sofia, June 2012, ISBN: 978-954-438-975-8.

[2] Lubomir Bogdanov, Hristo Nikolov, and **Todor Stefanov**,
"Embedded Multi-Processor Systems-on-Chip",
First Edition published by Publishing House of TU-Sofia, April 2013, ISBN: 978-619-167-034-5.

International Journal Papers (peer reviewed)

[3] Teddy Zhai, Hristo Nikolov, and **Todor Stefanov**,
"Mapping of Streaming Applications considering Alternative Application Specifications",
ACM Transactions on Embedded Computing Systems (TECS), vol. 12, Issue 1s, Article 34, March 2013.

[4] Mohamed A. Bamakhrama and **Todor Stefanov**,
"On the Hard-Real-Time Scheduling of Embedded Streaming Applications",
Accepted for publication in International Journal on Design Automation for Embedded Systems (DAES), June 2012 (in press, available on-line at http://dx.doi.org/10.1007/s10617-012-9086-x).

[5] Dmitry Nadezhkin, Hristo Nikolov, and **Todor Stefanov**,
"Automated Generation of Polyhedral Process Networks from Programs with Dynamic Loop Bounds"
Accepted for publication in ACM Transactions on Embedded Computing Systems (TECS), June 2012.

[6] Emanuele Cannella, Onur Derin, Paolo Meloni, Giuseppe Tuveri, and **Todor Stefanov**,
"Adaptivity Support for MPSoCs based on Process Migration in Polyhedral Process Networks",
International Journal of VLSI Design, vol. 2012, Article ID 987209, 17 pages, 2012.

[7] Jae Young Hur, Stephan Wong, and **Todor Stefanov**,
"Customization of On-Chip Network Interconnects and Experiments in FPGAs",
IET Computers & Digital Techniques Journal, vol. 6, Issue 1, pp. 59 - 68, Jan 2012.

[8] Jae Young Hur, Stephan Wong, and **Todor Stefanov**,
"Design Trade-offs in Customized On-Chip Crossbar Schedulers",
Journal of Signal Processing Systems (JVLSI), vol. 58, No. 1, pp. 69-85, Jan 2010.

[9] A. Gerstlauer, C. Haubelt, A.D. Pimentel, **Todor Stefanov**, D.D. Gajski, and J. Teich,
"Electronic System-Level Synthesis Methodologies",
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 28, No. 10, pp. 1517-1530, Oct 2009.

[10] Ozana Silvia Dragomir, **Todor Stefanov**, and Koen Bertels,
"Optimal Loop Unrolling and Shifting for Reconfigurable Architectures",
ACM Transactions on Reconfigurable Technology and Systems (TRETS), vol. 2, No. 4, pp. 1-24, Sept 2009.

[11] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
"Automated Integration of Dedicated Hardwired IP Cores in Heterogeneous MPSoCs Designed with ESPAM",
EURASIP Journal on Embedded Systems, vol. 2008, Article ID 726096, 15 pages, 2008.
doi:10.1155/2008/726096.

[12] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
"Systematic and Automated Multi-processor System Design, Programming, and Implementation",
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, No. 3, pp. 542-555, March 2008.
WINNER of the 2009 DONALD O. PEDERSON BEST PAPER AWARD!
(http://tcad.polito.it/editor/best_paper_award.html)
TOP 10th downloaded article of the IEEE TCAD for 2009!
(http://tcad.polito.it/editor/Top_2009CAD.html)
TOP 7th downloaded article of the IEEE TCAD for 2008!
(http://tcad.polito.it/editor/Top_2008CAD.html)

[13] Sven Verdoolaege, Hristo Nikolov, and **Todor Stefanov**,
"PN: a Tool for Improved Derivation of Process Networks",
EURASIP Journal on Embedded Systems, vol. 2007, Article ID 75947, 13 pages, 2007. doi:10.1155/2007/75947.

[14] **Todor Stefanov** (with P. Manoilov, G.Kousmanov and A. Popov),
"Development of a Low Area Custom Microprocessor Core",
Automatica & Informatics Journal, 1999. No. 5, pp. 33-39

International Conference Papers (peer reviewed)

[15] Jelena Spasic and **Todor Stefanov**,
"An Accurate Energy Model for Streaming Applications Mapped on MPSoC Platforms",
In Proc. "13th IEEE Int. Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation (IC-SAMOS'13)", pp., Samos, Greece, July 15-18, 2013.

[16] Teddy Zhai, Mohamed Bamakhrama, and **Todor Stefanov**,
"Exploiting Just-enough Parallelism when Mapping Streaming Applications in Hard Real-time Systems",
In Proc. "50th ACM/IEEE Int. Design Automation Conference (DAC'13)", pp., Austin, TX, USA, June 2-6, 2013.
WINNER of the 2013 HiPEAC PAPER AWARD!

[17] Sven Verdoolaege, Hristo Nikolov, and **Todor Stefanov**,
"On Demand Parametric Array Dataflow Analysis",
In Proc. "3rd International Workshop on Polyhedral Compilation Techniques (IMPACT'13)", Berlin, Germany, Jan. 21, 2013.

[18] Teddy Zhai, Hristo Nikolov, and **Todor Stefanov**,
"Mapping Streaming Applications considering Alternative Application Specifications (Extended Abstract)",
In Proc. "10th Int. IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia'12)", Tampere, Finland, Oct. 11-12, 2012.

[19] Mohamed A. Bamakhrama, and **Todor Stefanov**,
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In Proc. "10th IEEE/ACM/IFIP Int. Conf. on HW/SW Codesign and System Synthesis (CODES+ISSS'12)", pp. 83-92, Tampere, Finland, Oct. 7-12, 2012.

[20] Paolo Meloni, Giuseppe Tuveri, Luigi Raffo, Emanuele Cannella, **Todor Stefanov**, Onur Derin, Leandro Fiorin and Mariagiovanna Sami,
"System Adaptivity and Fault-tolerance in NoC-based MPSoCs: the MADNESS Project Approach",
to appear In Proc. "15th Euromicro Conf. on Digital System Design (DSD'12)", pp. , Izmir, Turkey, Sept. 5-8, 2012.

[21] Mohamed A. Bamakhrama, Teddy Zhai, Hristo Nikolov, and **Todor Stefanov**,

"A Methodology for Automated Design of Hard-Real-Time Embedded Streaming Systems",
In Proc. "15th Int. Conf. Design, Automation and Test in Europe (DATE'12)", pp. 941-946, Dresden, Germany, Mar. 12-16, 2012.

[22] Emanuele Cannella, Onur Derin, and **Todor Stefanov**,
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In Proc. "Int. Conf. on Design and Architectures for Signal and Image Processing (DASIP'11)", pp. , Tampere, Finland, Nov. 2-4, 2011.

[23] Dmitry Nadezhkin and **Todor Stefanov**
"Automatic Derivation of Polyhedral Process Networks from While-Loop Affine Programs",
In Proc. "9th Int. IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia'11)", pp. 102-111, Taipei, Taiwan, Oct. 13-14, 2011.

[24] Mohamed A. Bamakhrama and **Todor Stefanov**,
"Hard-Real-Time Scheduling of Data-Dependent Tasks in Embedded Streaming Applications",
In Proc. "11th International Conference on Embedded Software (EMSOFT'11)", pp. 195-204, Taipei, Taiwan, Oct. 9-14, 2011.
NOMINATED for the 2011 EMSOFT BEST PAPER AWARD!

[25] Razvan Nane, Sven Van Haastregt, **Todor Stefanov**, Bart Kienhuis, Vlad Mihai Sima and KoenBertels,
"IP-XACT Extensions for Reconfigurable Computing",
In Proc. "22nd IEEE Int. Conf. on Application-specific Systems, Architectures and Processors (ASAP'11)", pp. , Santa Monica, California, USA, Sep. 11-14, 2011.

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In Proc. "48th ACM/IEEE Int. Design Automation Conference (DAC'11)", pp. 116-121, San Diego, CA, USA, June 5-9, 2011.
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[27] Dmitry Nadezhkin, Hristo Nikolov, and **Todor Stefanov**
"Translating Affine Nested-Loop Programs with Dynamic Loop Bounds into Polyhedral Process Networks",
In Proc. "8th Int. IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia'10)", pp. 21-30, Scottsdale, AZ, USA, Oct. 28-29, 2010.
WINNER of the 2010 ESTIMedia BEST PAPER AWARD!

[28] Sjoerd Meijer, Hristo Nikolov, and **Todor Stefanov**,
"Combining Process Splitting and Merging Transformations for Polyhedral Process Networks",
In Proc. "8th Int. IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia'10)", pp. 97-106, Scottsdale, AZ, USA, Oct. 28-29, 2010.

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In Proc. "10th Int. Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation (SAMOS'10)", pp. 372-379, Samos, Greece, July 19-22, 2010.

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"Throughput Modeling to Evaluate Process Merging Transformations in Polyhedral Process Networks",
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[31] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
"Run-time Reconfiguration of Polyhedral Process Networks Implementations",
In Proc. "17th Int. Conference on Advanced Computing and Communications (ADCOM'09)", pp. , Bangalore, India, Dec. 14-17, 2009.

[32] Zubair Nawaz, **Todor Stefanov**, and Koen Bertels,

"Efficient Hardware Generation for Dynamic Programming Problems",
In Proc. "International Conference on Field-Programmable Technology (FPT'09)", pp., Sydney, Australia, Dec. 9-11, 2009.

[33] Sjoerd Meijer, Hristo Nikolov, and **Todor Stefanov**,
"On Compile-time Evaluation of Process Partitioning Transformations for Kahn Process Networks",
In Proc. "7th IEEE/ACM/IFIP Int. Conf. on HW/SW Codesign and System Synthesis (CODES-ISSS'09)", pp. 31-40, Grenoble, France, Oct. 11-16, 2009.

[34] Dmitry Nadezhkin, Sjoerd Meijer, **Todor Stefanov**, and Ed Deprettere,
"Realizing FIFO Communication when Mapping Kahn Process Networks onto Cell",
In Proc. "9th Int. Symposium on Embedded Computer Systems: Architectures, MOdeling, and Simulation (SAMOS'09)", LNCS 5657, pp. 308-317, Samos, Greece, July 20-23, 2009.

[35] Zubair Nawaz, Thomas Marconi, Koen Bertels, and **Todor Stefanov**,
"Flexible Pipelining Design for Recursive Variable Expansion",
In Proc. "23rd IEEE International Symposium on Parallel and Distributed Processing (IPDPS'09)", pp. 1-8, Rome, Italy, May. 23-29, 2009.

[36] Ozana Silvia Dragomir, **Todor Stefanov**, and Koen Bertels,
"Loop Unrolling and Shifting for Reconfigurable Architectures",
In Proc. "18th Int. Conference on Field Programmable Logic and Applications (FPL'08)", pp. 167-172, Heidelberg, Germany, Sep. 8-10, 2008.

[37] Hristo Nikolov, Mark Thompson, **Todor Stefanov**, Andy Pimentel, Simon Polstra, Raj Bose, Claudiu Zissulescu, and Ed Deprettere,
"Daedalus: Toward Composable Multimedia MP-SoC Design",
Invited paper In Proc. "45th ACM/IEEE Int. Design Automation Conference (DAC'08)", pp. 574-579, Anaheim, USA, June 8-13, 2008.

[38] Andy Pimentel, **Todor Stefanov**, Hristo Nikolov, Mark Thompson, Simon Polstra, and Ed Deprettere,
"Tool Integration and Interoperability Challenges of a System-level Design Flow: a Case Study",
Invited paper In Proc. "8th Int. Symposium on Systems, Architectures, MOdeling, and Simulation (SAMOS'08)", LNCS 5114, pp. 167-176, Samos, Greece, July 21-24, 2008.

[39] Kamana Sigdel, Mark Thompson, Andy Pimentel, **Todor Stefanov**, and Koen Bertels,
"System Level Design Space Exploration of Dynamic Reconfigurable Architectures",
In Proc. "8th Int. Symposium on Systems, Architectures, MOdeling, and Simulation (SAMOS'08)", LNCS 5114, pp. 279-288, Samos, Greece, July 21-24, 2008.

[40] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
"Parameterized Stream-Based Functions Model of Computation",
In Proc. "6th Int. Workshop on Optimizations for DSP and Embedded Systems (ODES-6)", pp., Boston, USA, April 6, 2008.

[41] Mark Thompson, Hristo Nikolov, **Todor Stefanov**, Andy Pimentel, Cagkan Erbas, Simon Polstra, and Ed Deprettere,
"A Framework for Rapid System-level Exploration, Synthesis, and Programming of Multimedia MP-SoCs",
In Proc. "5th IEEE/ACM/IFIP Int. Conf. on HW/SW Codesign and System Synthesis (CODES-ISSS'07)", pp. 9-14, Salzburg, Austria, Oct. 1-5, 2007.

[42] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
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In Proc. "17th Int. Conference on Field Programmable Logic and Applications (FPL'07)", pp. 580-584, Amsterdam, The Netherlands, Aug. 27-29, 2007.

[43] Jae Young Hur, **Todor Stefanov**, Stephan Wong, and Stamatis Vassiliadis,
"Customizing Reconfigurable On-Chip Crossbar Scheduler",
In Proc. "18th IEEE Int. Conf. on Application-specific Systems, Architectures and Processors (ASAP'07)", pp. 210-215, Montreal, Quebec, Canada, July 9-11, 2007.

[44] Kai Huang, Lothar Thiele, **Todor Stefanov**, and Ed Deprettere,
"Performance Analysis of Multimedia Applications using Correlated Streams",
In Proc. "10th Int. Conf. Design, Automation and Test in Europe (DATE'07)", pp. 912-917, Acropolis, Nice, France, Apr. 16-20, 2007.

[45] Jae Young Hur, **Todor Stefanov**, Stephan Wong, and Stamatis Vassiliadis,
"Systematic Customization of On-Chip Crossbar Interconnects",
In Proc. "International Workshop on Applied Reconfigurable Computing (ARC'07)", pp. 61-72, Mangaratiba, Rio de Janeiro, Brazil, Mar. 27-29, 2007,
In LNCS 4419, see the publisher version.

[46] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
"Multi-processor System Design with ESPAM",
In Proc. "4th IEEE/ACM/IFIP Int. Conf. on HW/SW Codesign and System Synthesis (CODES-ISSS'06)", pp. 211-216, Seoul, Korea, Oct. 22-25, 2006.
The most highly-cited CODES/ISSS paper for 2006!
(http://portal.acm.org/citation.cfm?id=1450178

[47] Ed Deprettere, **Todor Stefanov**, Shuvra Bhattacharyya, and Mainak Sen,
"Affine Nested Loop Programs and their Binary Parameterized Dataflow Graph Counterparts",
In Proc. "17th IEEE Int. Conf. on Application-specific Systems, Architectures and Processors (ASAP'06)", pp. 186-190, Steamboat Springs, Colorado, USA, Sep. 11-13, 2006.

[48] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
"Efficient Automated Synthesis, Programming, and Implementation of Multi-processor Platforms on FPGA Chips",
In Proc. "16th Int. Conference on Field Programmable Logic and Applications (FPL'06)", pp. 323-328, Madrid, Spain, Aug. 28-30, 2006.

[49] Sven Verdoolaege, Hristo Nikolov, and **Todor Stefanov**,
"Improved Derivation of Process Networks",
In Proc. "4th Int. Workshop on Optimizations for DSP and Embedded Systems (ODES'06)", pp., New York, NY, USA, Mar. 26, 2006.

[50] Hristo Nikolov, **Todor Stefanov**, and Ed Deprettere,
"Modeling and FPGA Implementation of Applications using Parameterized Process Networks with Non-Static Parameters",
In Proc. "13th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'05)", pp. 255-263, Napa, California, USA, Apr. 18-20, 2005.

[51] **Todor Stefanov**, Claudiu Zissulescu, Alexandru Turjan, Bart Kienhuis, and Ed Deprettere,
"System Design using Kahn Process Networks: The Compaan/Laura Approach",
In Proc. "7th Int. Conf. Design, Automation and Test in Europe (DATE'04)", pp. 340-345, Paris, France, Feb. 16-20, 2004.

[52] **Todor Stefanov** and Ed Deprettere,
"Deriving Process Networks from Weakly Dynamic Applications in System-Level Design",
In Proc. "IEEE/ACM/IFIP Int. Conf. on HW/SW Codesign and System Synthesis (CODES-ISSS'03)", pp. 90-96, Newport Beach, California, USA, Oct. 1-3, 2003.

[53] Ed Deprettere, **Todor Stefanov**, and Bart Kienhuis,
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In Proc."17th Int. Conf. on Systems for Automation of Engineering and Research (SAER'03)", pp. 18-26, St. Konstantin resort, Varna, Bulgaria, Sep. 19-21, 2003.

[54] Claudiu Zissulescu, **Todor Stefanov**, Bart Kienhuis, and Ed Deprettere,
"LAURA: Leiden Architecture Research and Exploration Tool",
In Proc. "13th Int. Conference on Field Programmable Logic and Applications (FPL'03)", pp. 911-920, Lisbon, Portugal, Sep. 1-3, 2003,
In LNCS 2778, see the publisher version.

[55] **Todor Stefanov**, Bart Kienhuis, and Ed Deprettere,

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In Proc."10th Int. Symposium on Hardware/Software Codesign (CODES'02)", pp. 7-12, Estes Park, Colorado, USA, May 6-8, 2002.

[56] Alexandru Turjan, **Todor Stefanov**, Bart Kienhuis, and Ed Deprettere,
"The COMPAAN Tool Chain to convert Matlab into Process Networks",
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[57] Tim Harriss, Richard Walke, **Todor Stefanov**, Alexandru Turjan, Bart Kienhuis, and Ed Deprettere,
"QR implementation onto an FPGA as part of a Beam former application",
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[58] **Todor Stefanov**, Paul Lieverse, Pieter van der Wolf, and Ed Deprettere,
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In Proc."IEEE/ACM Int. Conference on Computer Aided Design (ICCAD'01)", pp. 31-38, San Jose, California, USA, Nov. 4-8, 2001.

[59] **Todor Stefanov**, Ed Deprettere, and Bart Kienhuis,
"Exploring Application Model Instances in System-Level Design",
In Proc."Workshop on Embedded Systems (PROGRESS'01)", pp. 243-250, Veldhoven, The Netherlands, Oct. 18, 2001.

[60] **Todor Stefanov,** Paul Lieverse, Ed Deprettere, and Pieter van der Wolf,
"Y-Chart Based System Level Performance Analysis: An M-JPEG Case Study",
In Proc."Workshop on Embedded Systems (PROGRESS'00)", pp. 129-140, Utrecht, The Netherlands, Oct. 13, 2000.

[61] **Todor Stefanov** (with P. Manoilov, G.Kousmanov and A. Popov),
"Two Approaches in One for a Quick and Efficient Design of Low Area Custom Microprocessor Cores",
In Proc. "Electronics '98", Sozopol, Bulgaria, Sep. 1998.

Appendix B

Citation Analysis Data